Abstract of the Disclosure

Disclosed is a multiprocessor system including a semaphore register and a semaphore interrupt register. In addition, for each processor in the multiprocessor system, there is a semaphore interrupt enable register. If a first processor finds that a semaphore cell of the semaphore register holds a "1" indicating that an associated shared resource is being accessed by a second processor, the first processor sets a corresponding semaphore interrupt enable cell of the semaphore interrupt enable register to "1" so as to enable semaphore interrupt. When the second processor finishes with the shared resource, the second processor writes a 0 into the semaphore cell, causing a corresponding semaphore interrupt cell of the semaphore interrupt register to hold a "1". This, combined with the fact that the semaphore interrupt enable cell also holds a "1", causes an interrupt to the first processor. In response, the first processor services the interrupt and accesses the shared resource. As a result, repetitive reading and writing the semaphore cell by the first processor via a system bus of the multiprocessor system can be avoided.